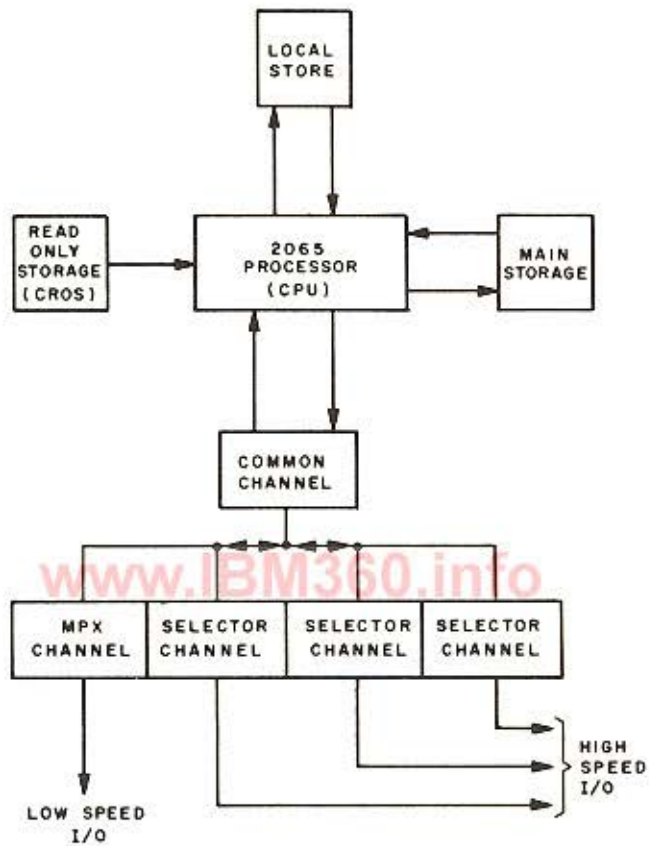


TABLE OF CONTENTS

<u>CROS AND TIMING</u>	<u>Figure No.</u>	<u>Page No.</u>
Basic Computer.....	1-1	1
CROS "Big Picture".....	1-2	2
CROS Hardware.....	1-3	3
ROS Timing.....	1-4	4
ROS Field Timing.....	1-5	5
CROS Access Scheme.....	1-6	6
Array Driver.....	1-7	7
Data Movement Scheme.....	1-8	8
Decode Micro-order PAL To B Reg.....	1-9	9
ROSDR Latch Timing.....	1-10	10
PAL To B Data Movement.....	1-11	11
PAL To B Reg Timing.....	1-12	12
Clock Formation.....	1-13	13
Machine Language Program.....	1-14	14
 <u>I-FETCH</u>		
Microprogram "Big Picture".....	2-1	15
9020 D CE Microprogram "Big Picture" (Detailed).....	2-2	16
Instruction Request During NEOP And BEOP.....	2-3	17
I-FETCH Sequencer 1.....	2-4	18
I-FETCH Sequencer 1 Timing.....	2-5	19
I-FETCH Sequencers 2 And 3.....	2-6	20
I-FETCH Sequencer Timing.....	2-7	21
Q Refill Exceptional Condition.....	2-8	22
Exception μ -Order For "Q" Refill Priority (ROS 034).....	2-9	23
Gating SDBO To Q Reg.....	2-10	24
Gating Q To R And Illustrating Effective R Bit 0.....	2-11	25
SPEC μ -Order (K31) Force ROS To 010.....	2-12	26
Gating IC Plus 8 To Parallel Adder To IC.....	2-13	27

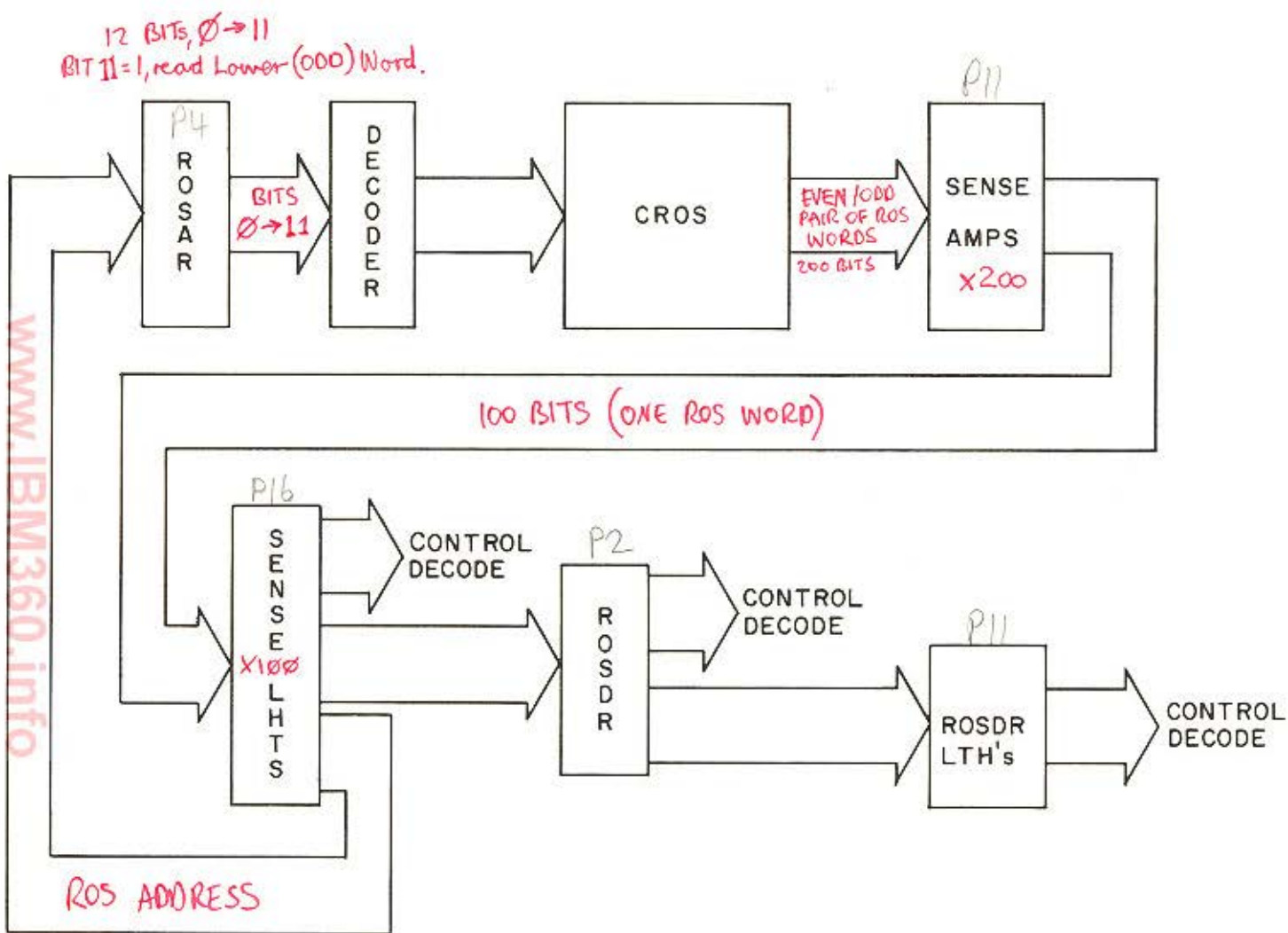
**LECTURE NOTES FROM THE FAA ACADEMY 9020 COURSE
"IBM 9020D/E SYSTEMS 7201-02 COMPUTING ELEMENT"
(ENHANCED IBM S/360 MODEL 65)**

**Coloured-in by Chris Bigos in Oklahoma USA 1979
Scanned in by Chris Bigos in London UK 2012**



Basic Computer

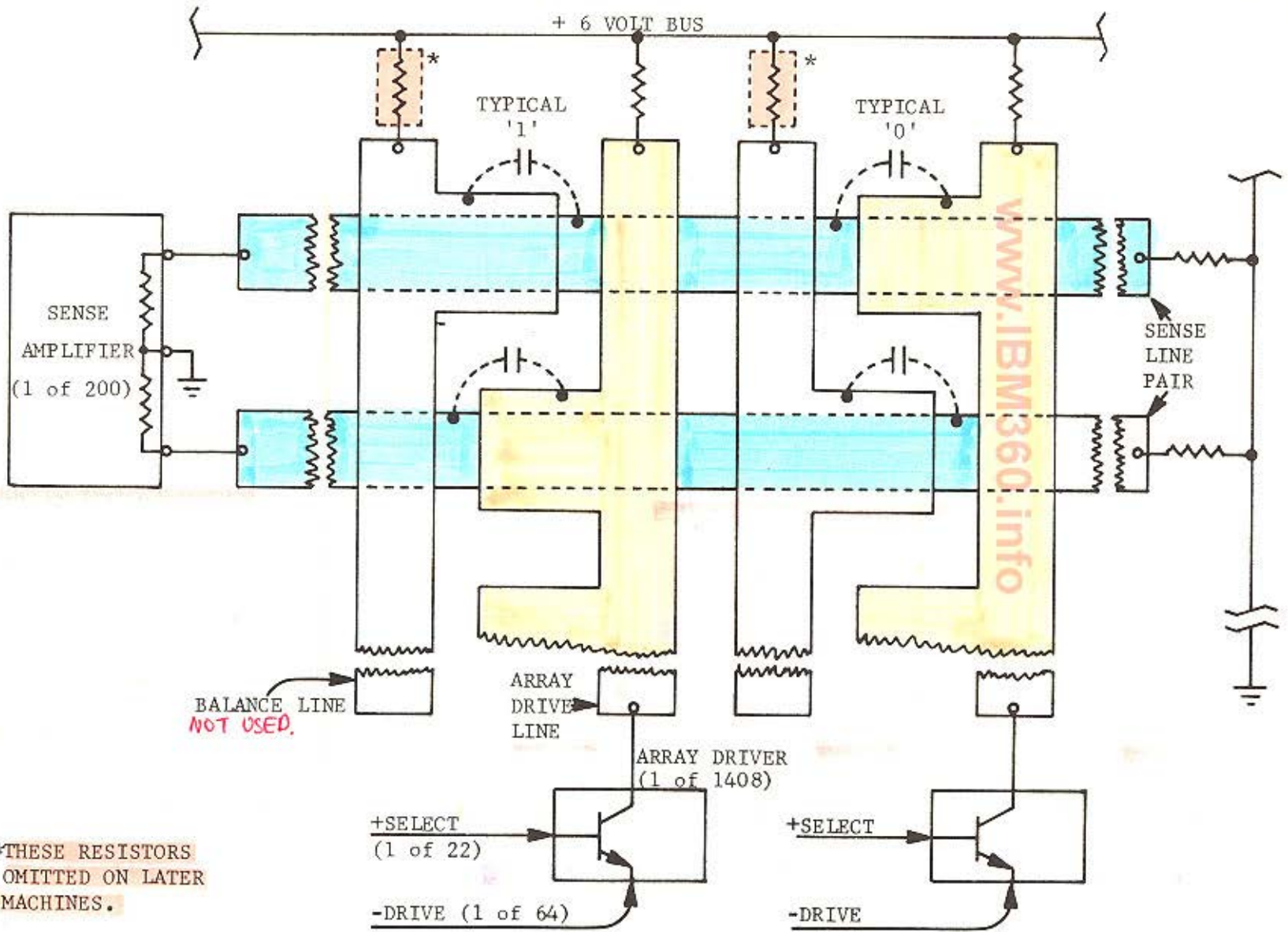
1-1



www.ibm360.info

2

CROS "Big Picture"



3

*THESE RESISTORS OMITTED ON LATER MACHINES.

CROS HARDWARE

SEE FETOM P2-10

WORD 0

WORD 1

WORD 2

P0 2 4 6 8 10 12 14 16 18 P0 2 4 6 8 10 12 14 16 18 P0 2 4 6 8 10 12 14 16 18

ROSAR

GATE DRIVER STROBE

GATE WORD SELECT STROBE

SENSE LATCH STROBE

SENSE LATCHES

ROSDR 2-42 INGATE REG.

ROSDR LATCHES

ROSDR 69-84 (OUTGATES)

ROSAR LATCHES

B CLOCK

P4-P3

P11-P17

P9-P18

P13-P18

P12-P16

P2-P1

P9-P8

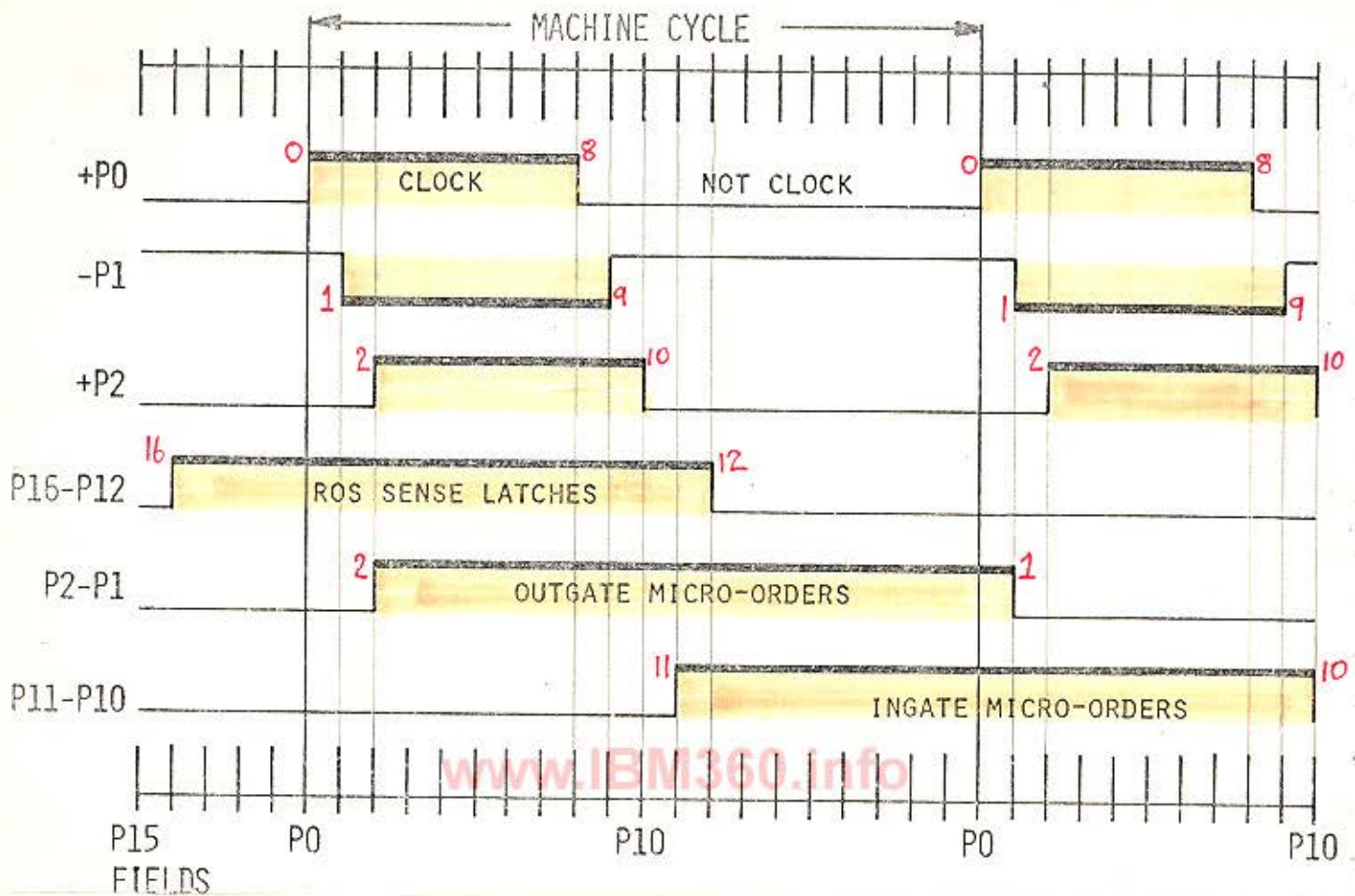
P2-P1

ROS TIMING See FETOM 1-27

1-4

www.ibm360.info

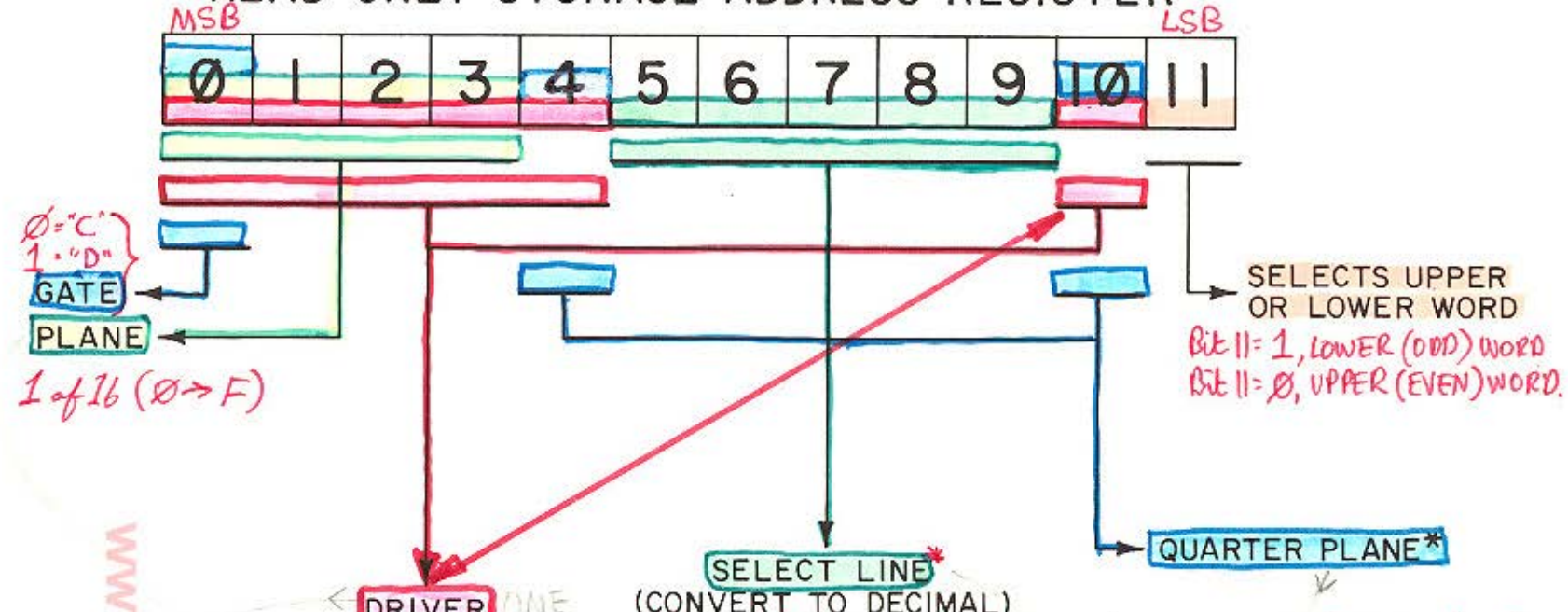
4



- | | | |
|---|---------------------|---------------------|
| A. P2-P1 (A7 ONLY)
P11-P10 (ALL OTHERS) | G. P2-P1
P11-P10 | P. P2-P1 |
| B. P11-P10 | H. P2-P1 | Q. P2-P1 |
| C. P2-P1 (C3 ONLY)
P11-P10 | L. P16-P12 | R. P2-P1 |
| D. P2-P1 (D1, D2, D3)
P11-P10 (ALL OTHERS) | NA. P16-P12 | T. P2-P1 |
| E. P2-P1
P11-P10 | J. P16-P12 | U. P2-P1 |
| F. P2-P1
P11-P10 | M. P2-P1 | V. P2-P1 |
| | N. P2-P1 | W. P2-P1
P11-P10 |

Any ROS address "XD8" → "XFF" is invalid. Any ROS address above "FD7" is invalid.

1 0 0 1 0 1 0 0 0 0 1 1 = X"943"
 READ ONLY STORAGE ADDRESS REGISTER



EG:- ADDR. "FAA"
 GATE - 1 = "D"
 PLANE - F = "15"
 DRIVER - 3F = "63"
 SEL. LINE - "A" = 10
 1/4 PLANE - "3"
 WORD - 0 = "UPPER"

www.IBM360.info

(CONVERT TO DECIMAL) *1 of 22 (0 → 21) Possible address range in bits 5 → 9 = "1F"
 "1F" = 31₁₀. Lines 22 → 31 are INVALID.
 *QUARTER PLANES ARE NUMBERED LEFT TO RIGHT FROM PRESSURE PLATE SIDE.

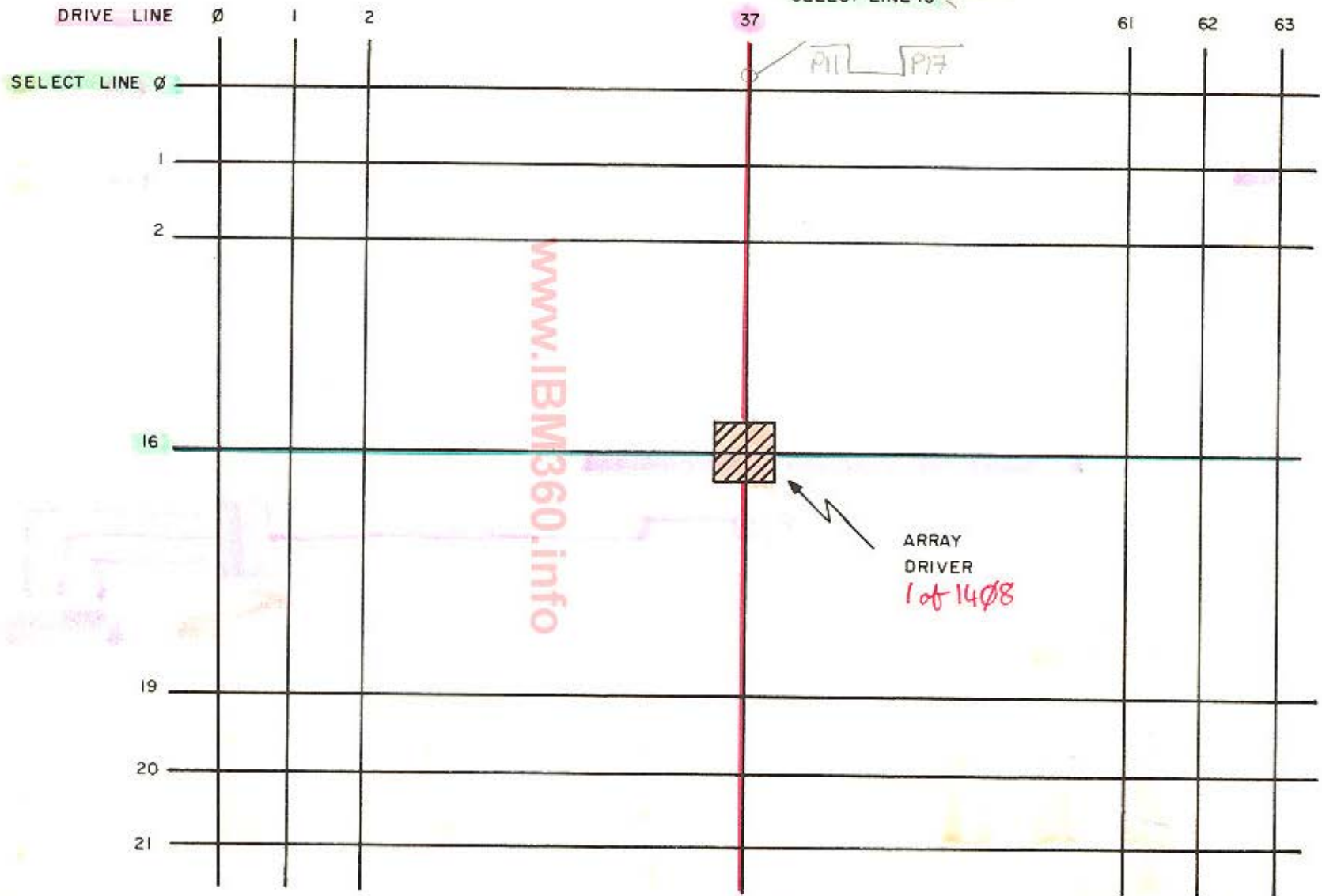
CROS ACCESS SCHEME

EXAMPLE CROSS WORD X '943'

DRIVE LINE 37, PLANE 9

QP 1

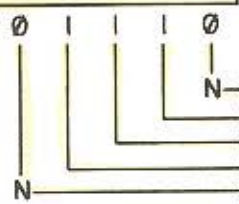
SELECT LINE 16



Array Driver
1-7

U FIELD (U14)

92 93 94 95 96 ROS SENSE LATCHES



ROS SENSE LATCHES

S 0-31 T 32-63

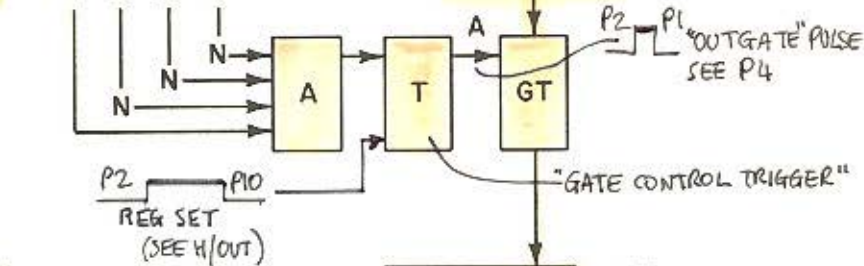
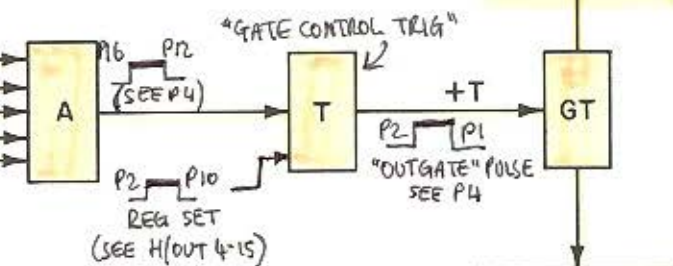
T FIELD (T8)

87 88 89 90 ROS SENSE LATCHES



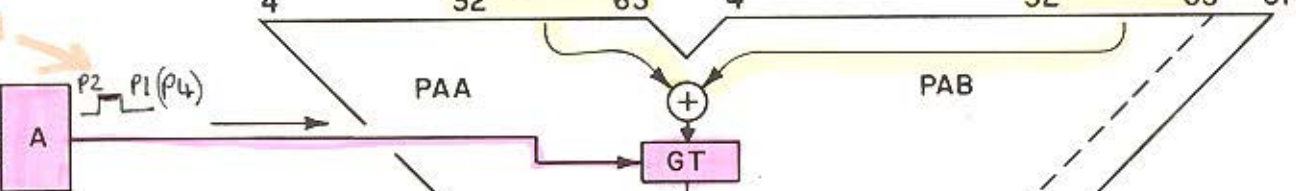
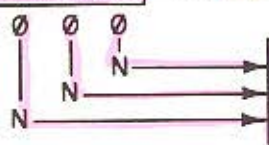
ROS SENSE LATCHES

A 0-31



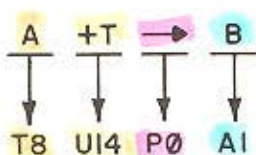
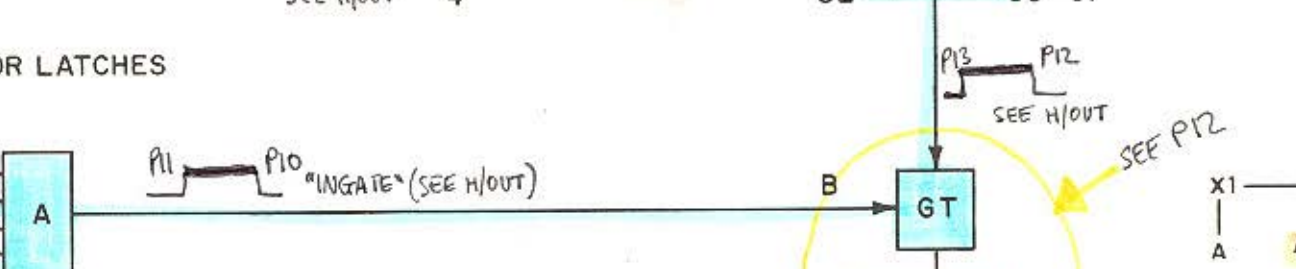
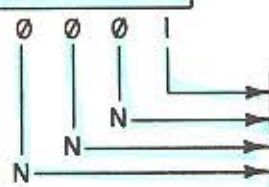
P FIELD (P0)

78 79 80 ROSDR



A FIELD (A1)

6 7 8 9 ROSDR LATCHES



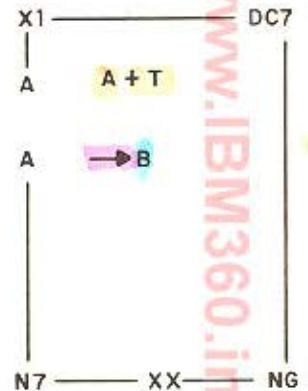
T8 - "A00-31 TO PB 32-63"
 U4 - "T32-63 TO PA32-63"
 P0 - "PADDER 04-67 TO PAL 04-67 (NO SHIFT)"
 A1 - "PAL 32-63 TO B 32-63"

DATA MOVEMENT SCHEME

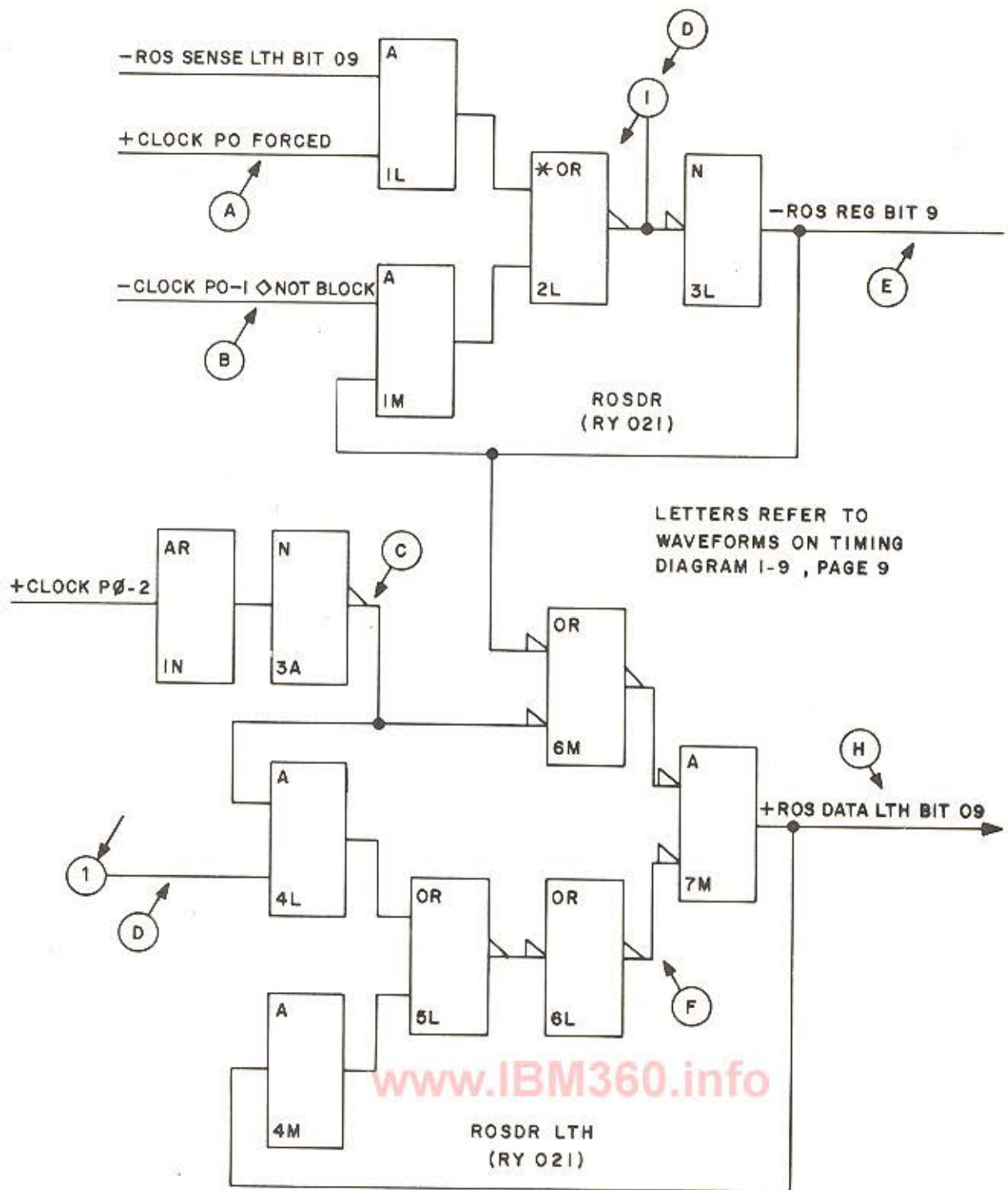
1-8

Timing on Handout 4-15.

REG RESET 10MS BEFORE "REG SET"

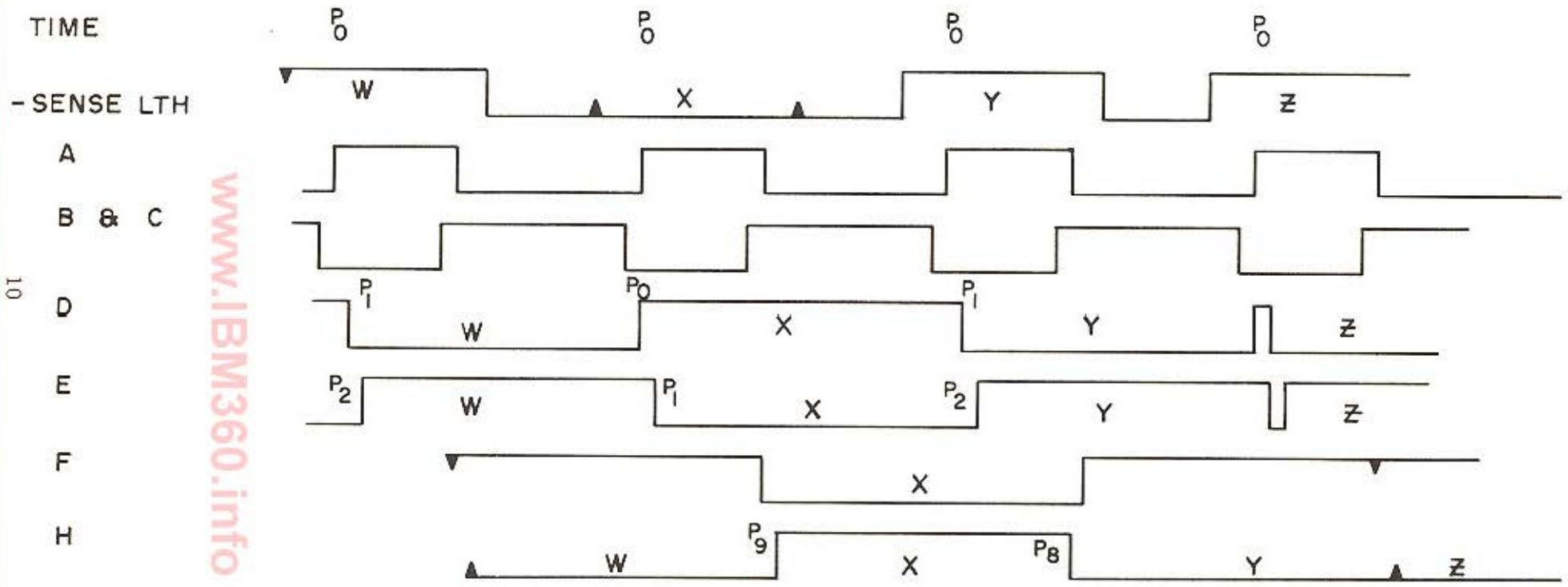


QQ 471



DECODE A1 MICRO - ORDER BIT 9
(GATE PAL TO B REG)

ROS WORD BIT
 W X Y Z
 ASSUME ROS SENSE LTH BIT 9 0 - 1 - 0 - 0



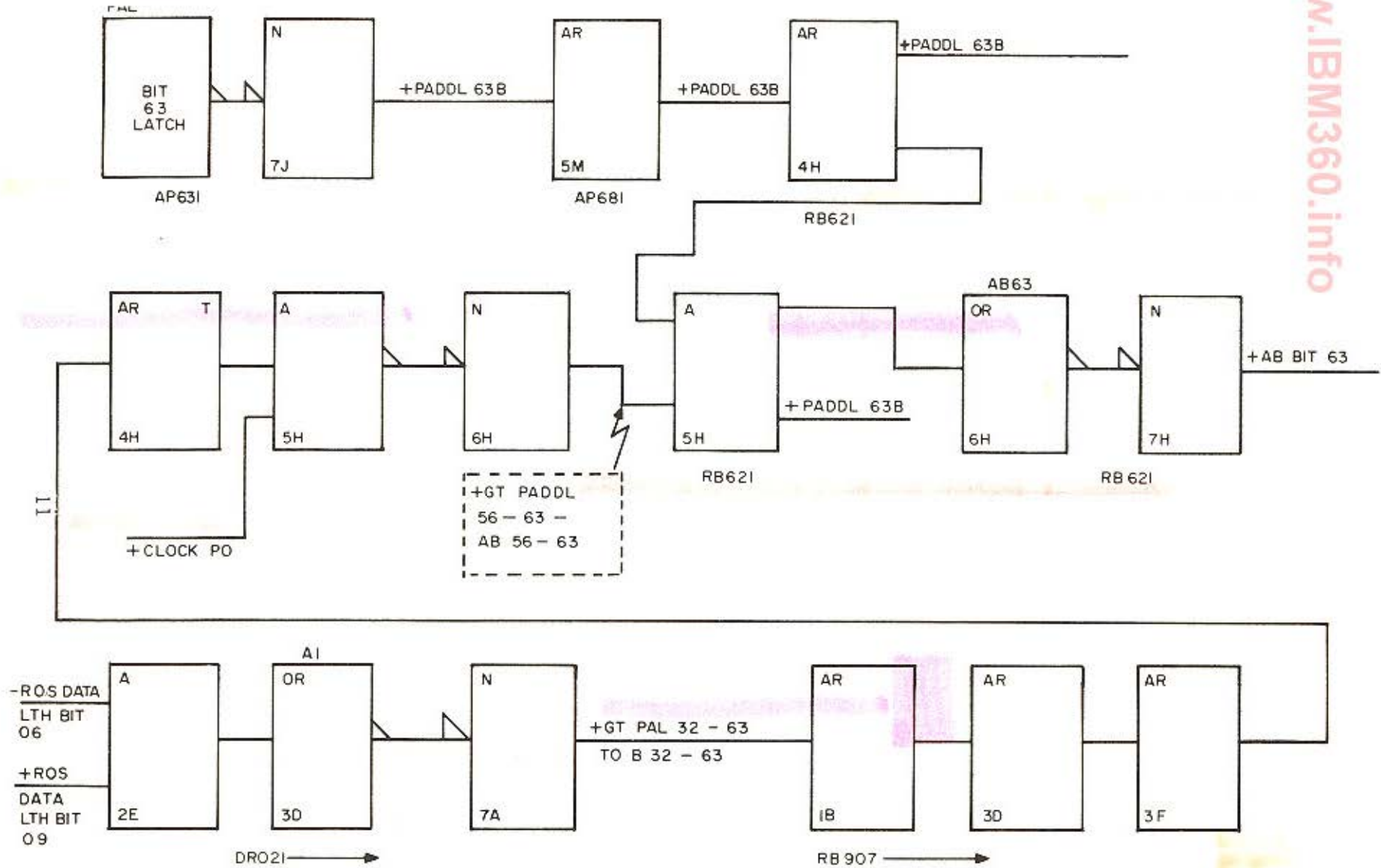
www.IBM360.info

FIG 1 - 9
LOCATIONS

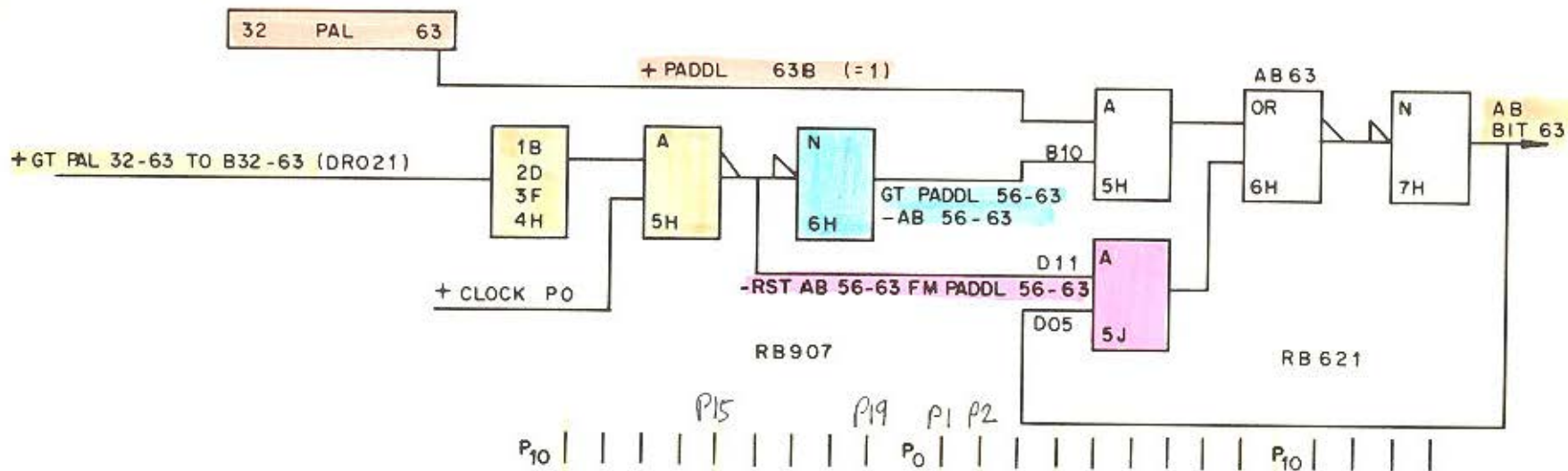
ROSDR - ROSDR LTH TIMING

1-10

www.ibm360.info



PAL to B Data Movement



+ PADDL 63B



12

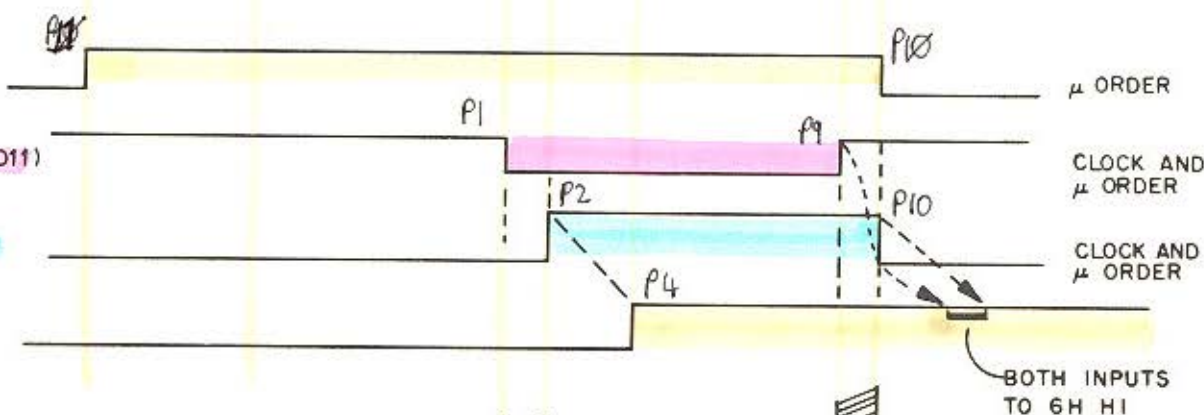
+ GT PAL 32-63 TO B 32-63

-RST AB 56-63 FM PADDL 56-63 5J (D11)

+ GT PADDL 56-63 - AB56-63 5H (B10)

+ AB BIT 63

5J (D05)

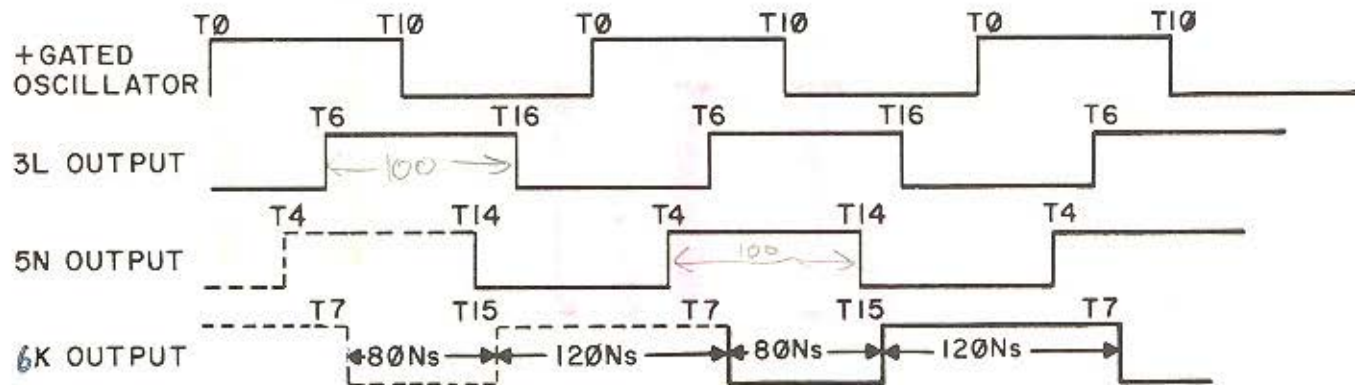
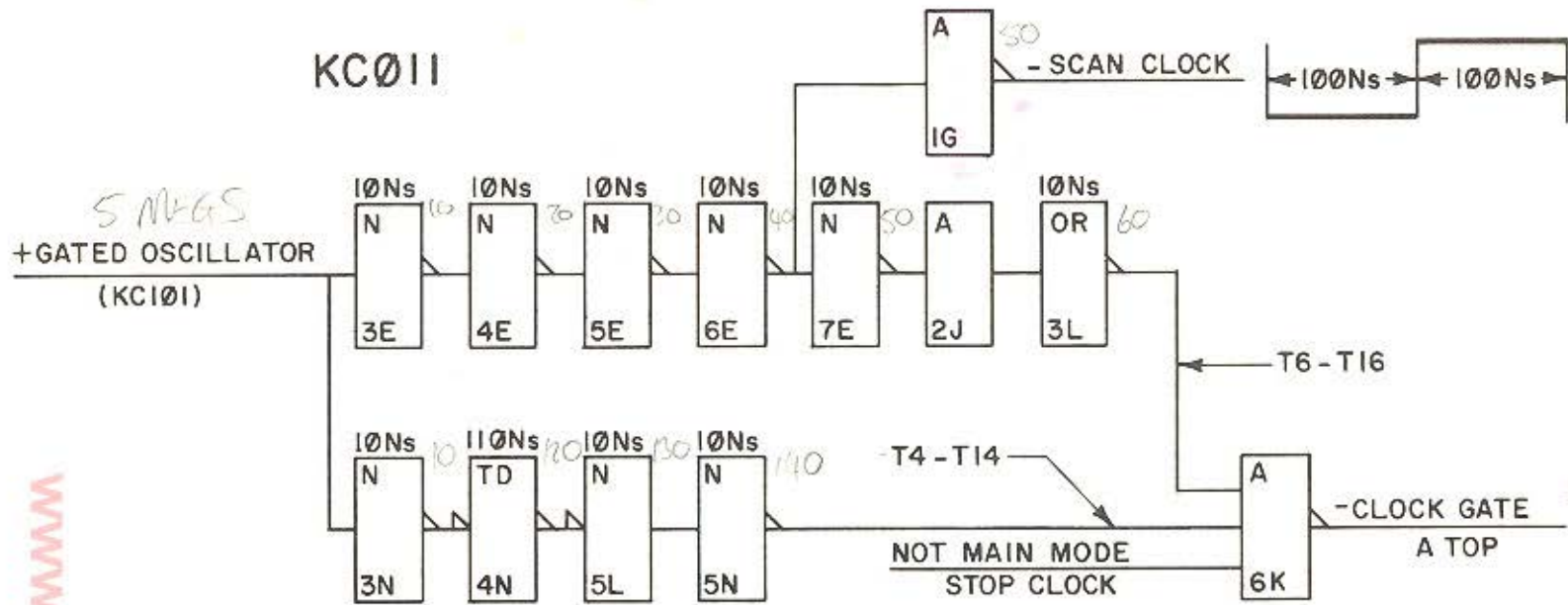


LATCH RESET
5H B10 & 5J D11
BOTH LOW

LATCH SET
5H B10 & 5J D11
BOTH HI
LATCH REMAINS
SET DUE TO HI
ON 5J D11 AND D05

PAL TO B REG TIMING

1-12 SEE P8



CLOCK FORMATION

MACHINE - LANGUAGE PROGRAM

www.IBM360.info

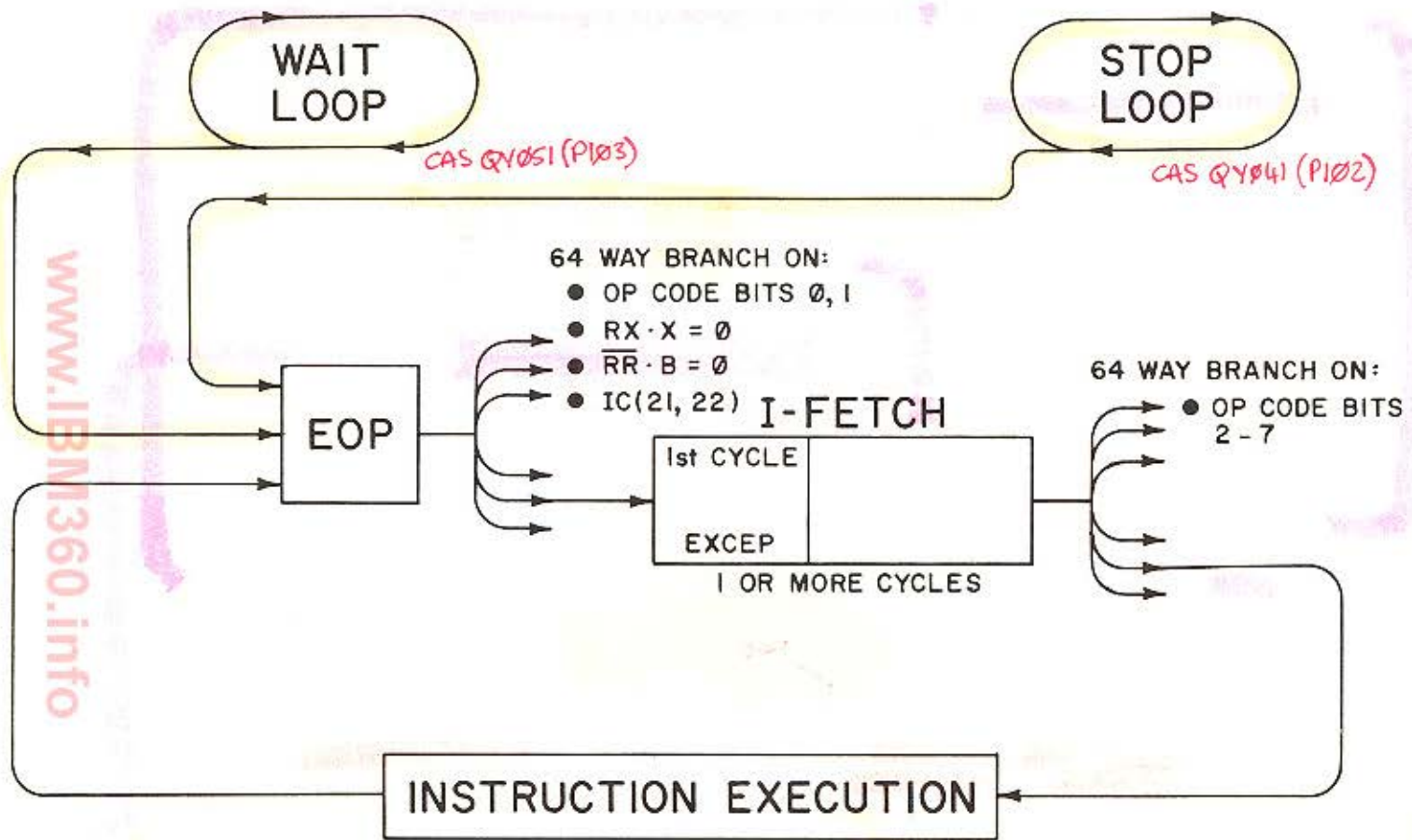
Storage Location

Data & Explanation of Data

IPSW LOC	IPSW	INST. ADR.
000000	X X X X X X X X	X X 0 0 1 0 0 0
001000	(BALR) R1 R2 (LM) R1 R3 0 5 6 0 9 8 0 5	B D I S (ST) R1 X 6 0 1 2 5 0 4 5
001008	B D I S (AP) L1 L2 6 0 2 A F A 2 1	B1 D I S B2 D I S 6 0 2 B 6 0 2 E
001010	(SCON) R1 R2 (SATR) R1 R2 0 1 2 4 0 D 0 1	Reg 0 (ATR 1 Msk) FOR SATR 4 3 1 2 0 0 0 0
001018	Reg 1 (ATR 2, Select) FOR SATR 0 0 0 0 0 0 4 2	Reg 2 (Config. Msk) FOR SCON A 0 F 0 0 4 0 2
001020	Reg 3 (Config. Msk) FOR SCON 0 0 0 0 0 0 0 0	Reg 4 (R1 for ST) FOR SCON (Select Msk) 0 0 F 0 0 4 0 2
001028	Reg 5 (X for ST) 0 0 0 0 0 0 0 8	AP Op 1 L1 FIELD - 3 BYTES 4 5 6 7 8 C
001030	AP Op 2 L2 FIELDS - 2 BYTES 7 8 9 C X X X X	Stor Wd for Reg 4 (ST) X X X X X X X X

SGN

Machine Language Program



MICROPROGRAM "BIG PICTURE"

J97: *

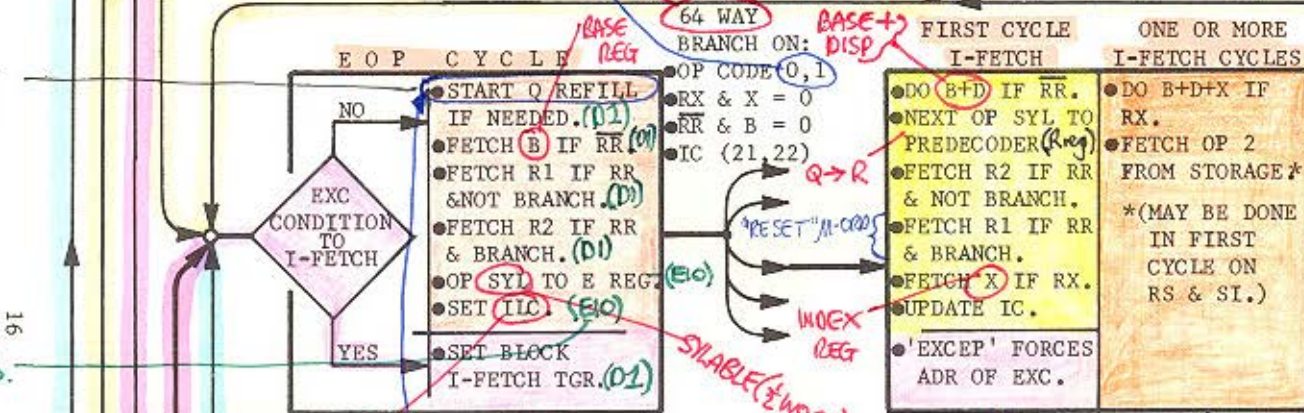
- ROSAR 6 IF R REG 0 = 1
- 7 IF R REG 1 = 2
- 8 IF RX + INDEX REG = 0
- 9 IF RR + BASE REG = 0
- 10 IF I.C. Bit 21 = 1
- 11 IF I.C. Bit 22 = 1.

0 0 1 - RR
0 0 0 - RX, RS, SI
1 0 1 - SS

SAME LOOP.



SEE NEXT PAGE



www.ibm360.info

- 64 WAY BRANCH ON:
- OP CODE BITS 2-7
- M-ORDER J103
- ROSAR 6 IF E2 = 1
 - 7 IF E3 = 1
 - 8 IF E4 = 1
 - 9 IF E5 = 1
 - 10 IF E6 = 1
 - 11 IF E7 = 1

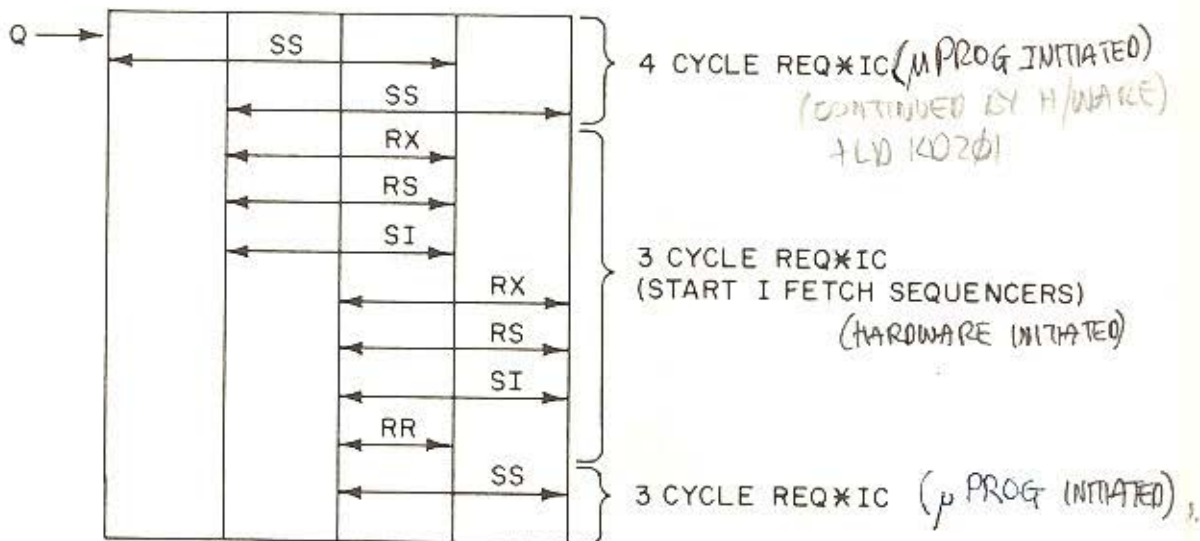
1 of up to 64 different routes. One for each type of instruction.

- EXCEPTION SERVICE RTNS
- WAIT BIT ON IN NEW PSW.
 - EXT OR MANUAL STOP.
 - ALL INTRPTS BUT CE ERROR.
 - Q REFILL IN PROGRESS.
 - ALL OTHER EXCEPTIONS.

- INSTRUCTION EXECUTION RTNS
- PERFORM ARITHMETIC OR LOGICAL FUNCTION PER OP CODE.
 - STORE RESULT.
 - SET CONDITION CODE.*
 - *(MAY BE DONE NEXT EOP CYCLE.)

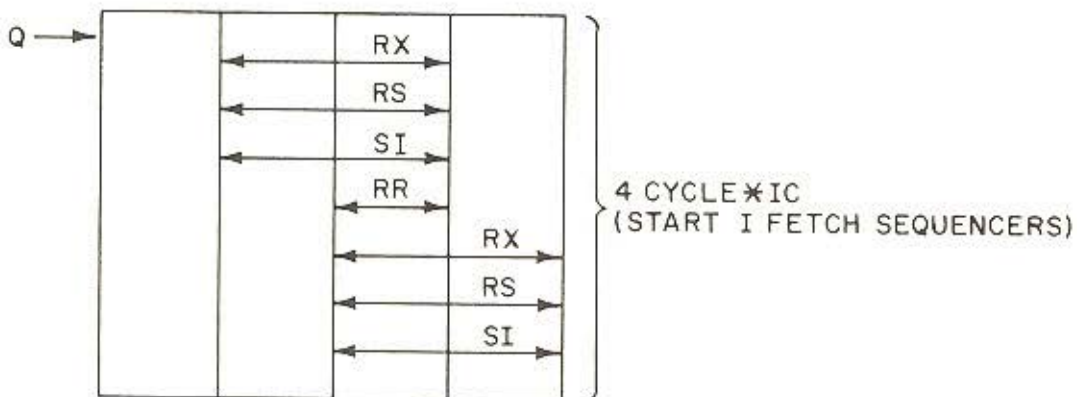
INSTRUCTION REQUEST DURING NEOP OR BEOP
 (NOT BRANCH INSTRUCTIONS OR EXECUTE NOT
 IN PROGRESS) REF: FEMDM 5-2, 5-30

IC (21-22) → 00 01 10 11



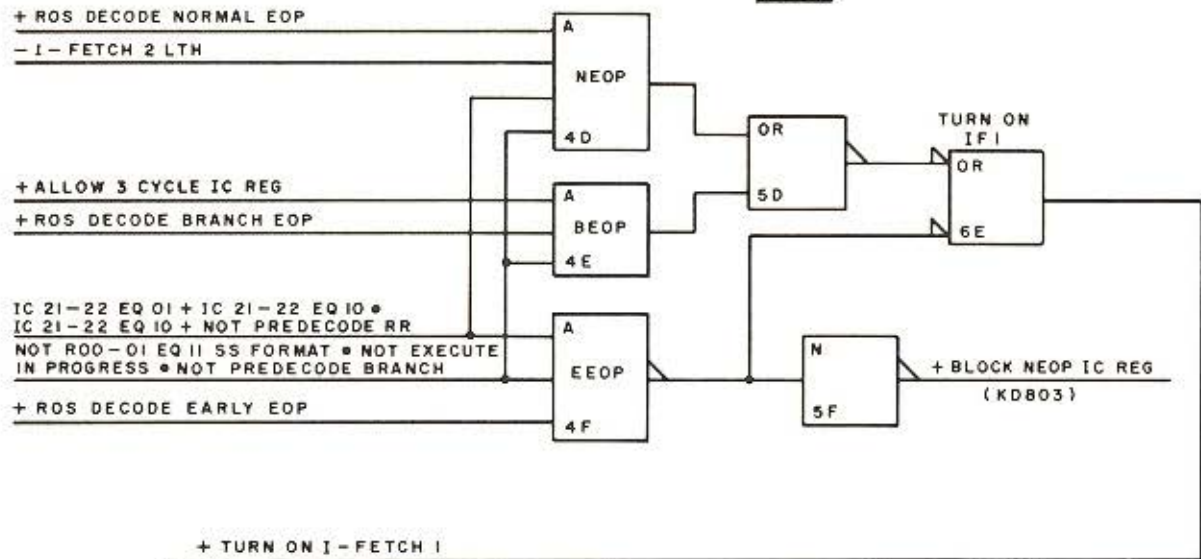
INSTRUCTION REQUEST DURING EEOP
 (NOT BRANCH INSTRUCTIONS OR EXECUTE
 NOT IN PROGRESS) REF: FEMDN 5-3, 5-30

IC (21-22) → 00 01 10 11

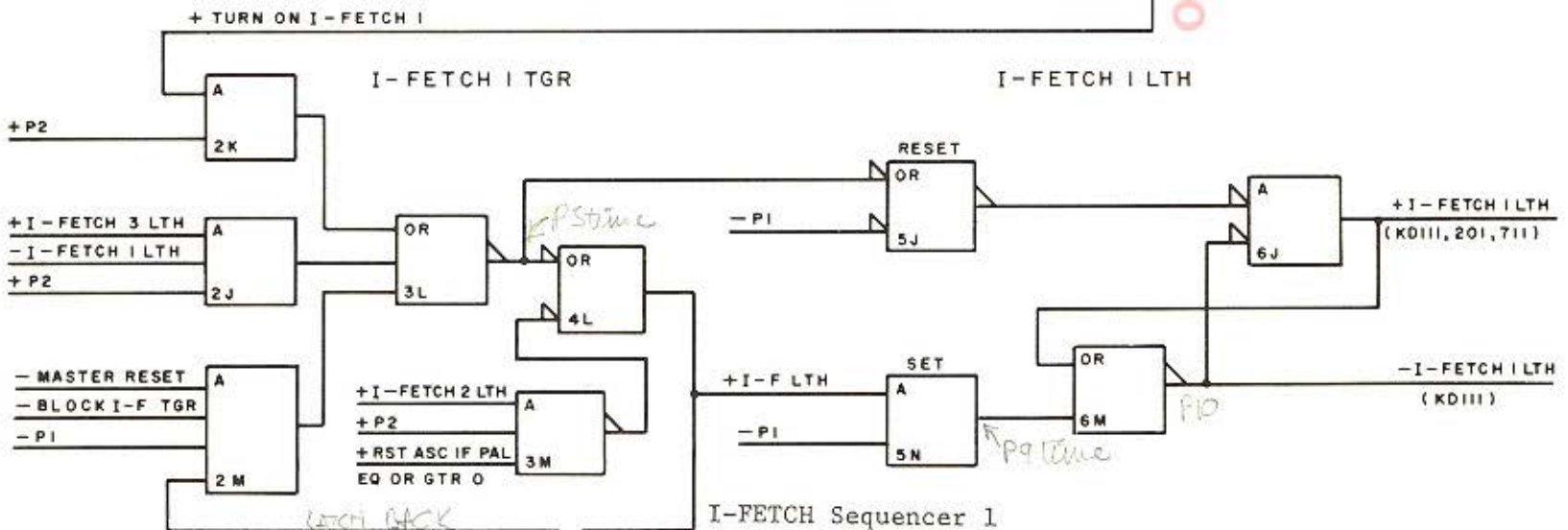


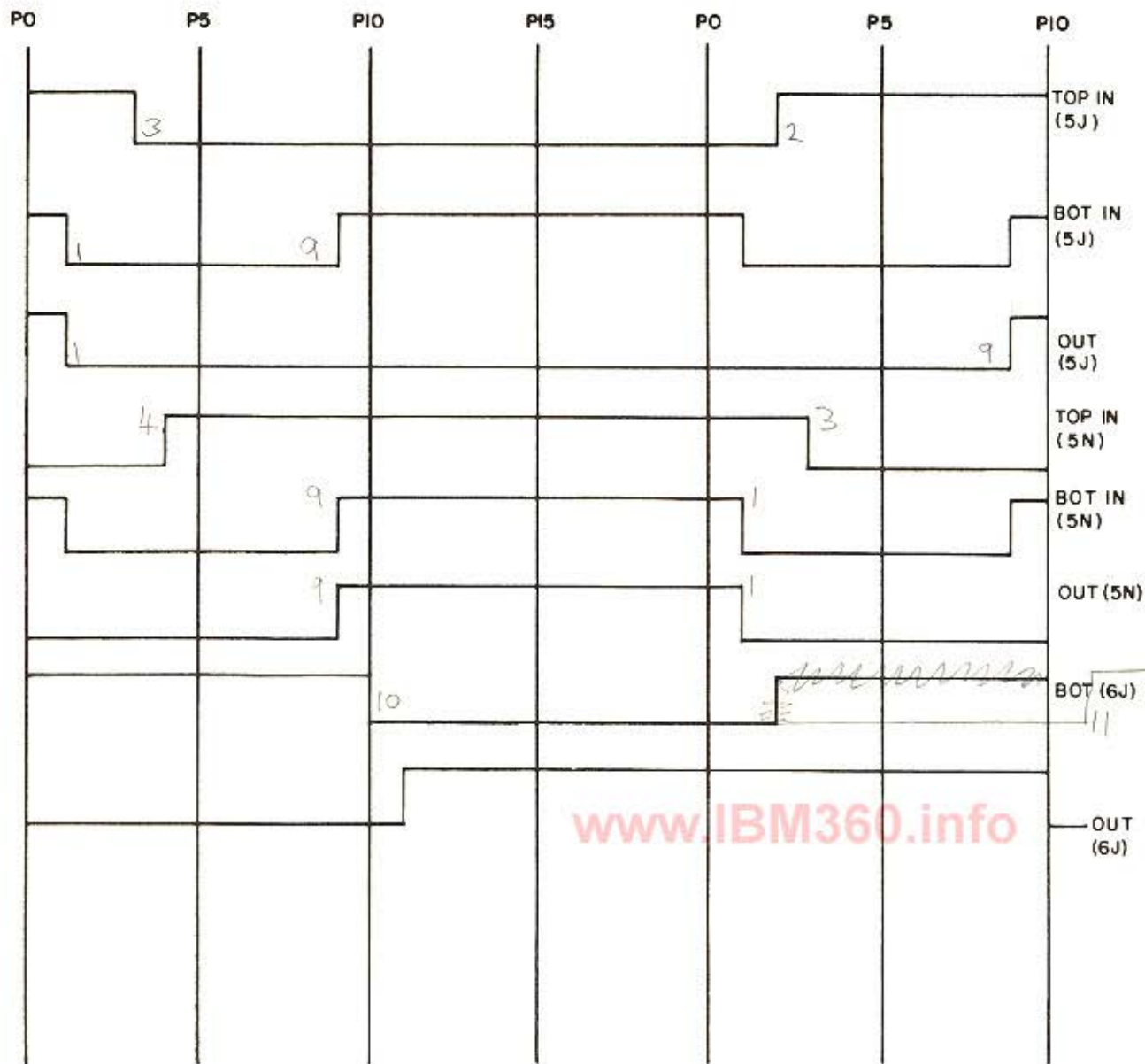
Instruction Request During NEOP and BEOP

KD101



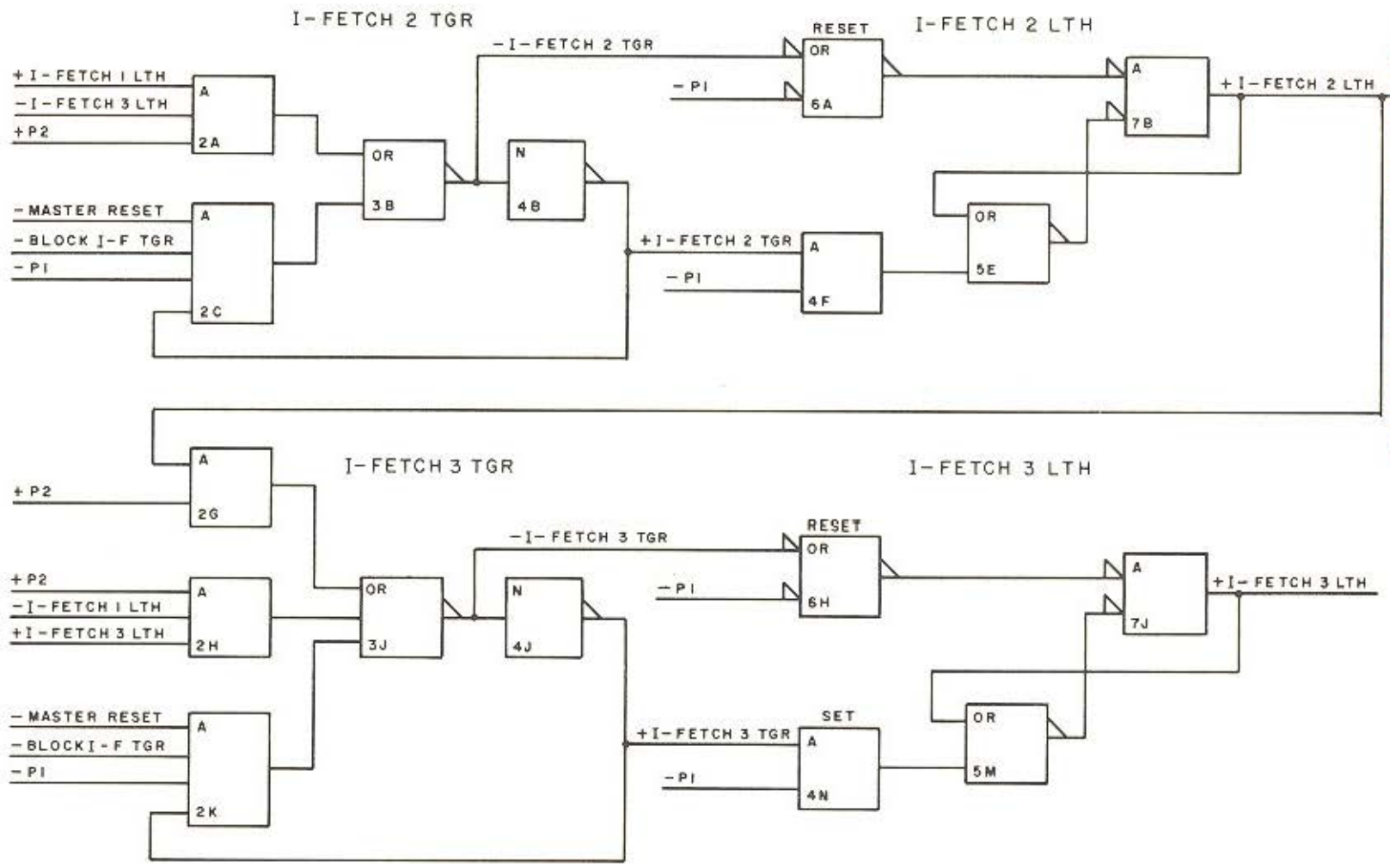
18





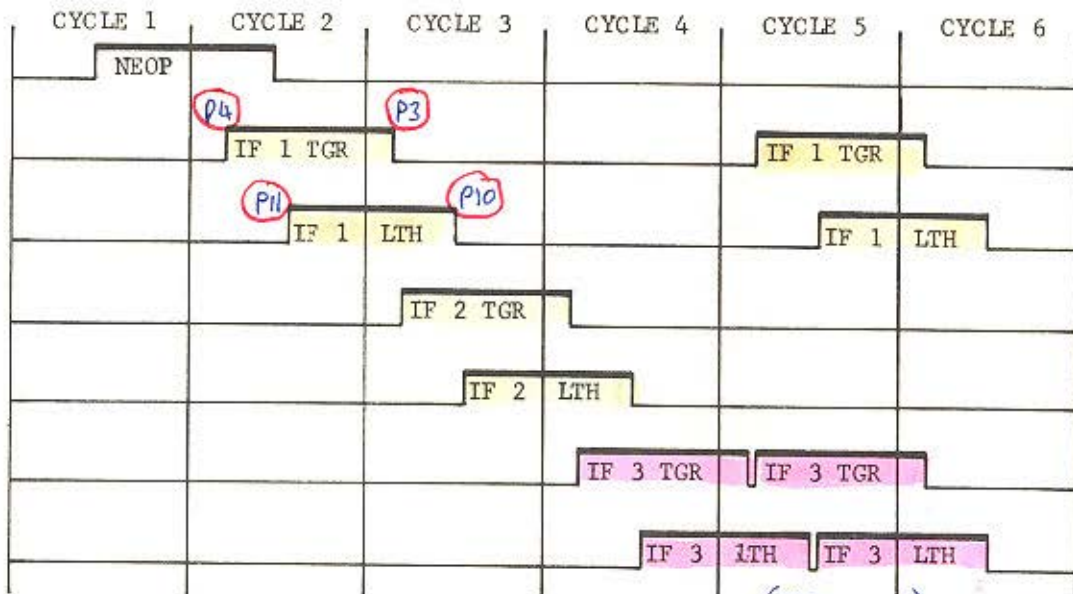
I-FETCH Sequencer 1 Timing

2-5

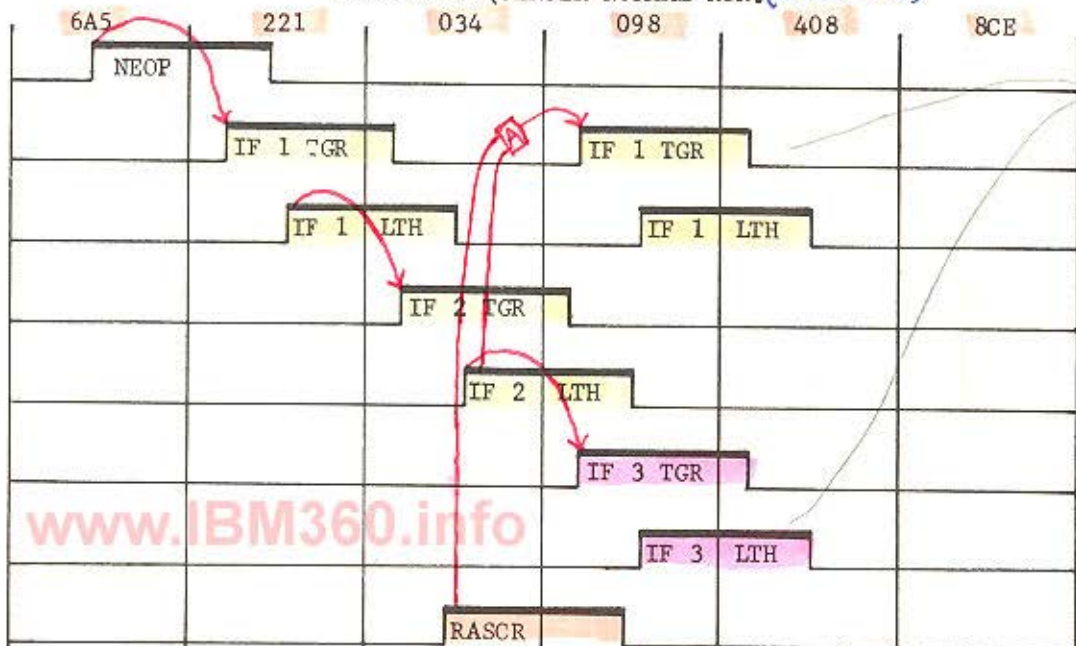


20

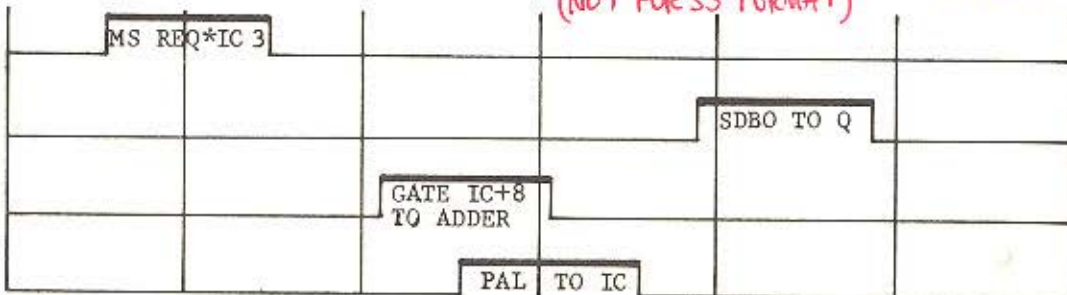
I-Fetch Sequencers 2 and 3



I-FETCH SEQUENCER NORMAL RUN. (EARLY EOP)



I-FETCH SEQUENCER RUN FORESHORTENED BY RASCR M-ORDER. (NEOP + BEOP)
(NOT FOR SS FORMAT)



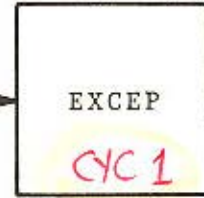
2-7 See next page. + DE-C-02 P93

6A5 (QE041)



I-FETCH

221 (QT005)



BY HARDWARE

034 (QT041)



- P18 1. HARDWARE DETECTS Q REFILL PRIORITY.
- P18 2. ISSUE 3-CYCLE REQUEST PER IC.
- P23 3. START I-FETCH SEQUENCERS. - DEC-02 P93
- P23 4. SET UP EXCEPTIONAL CONDITION TO I-FETCH.

- 1. BLOCK μ -ORDER E(02-07) \rightarrow ROA.
- 2. EXCEP μ -ORDER FORCES ROSAR TO 034.

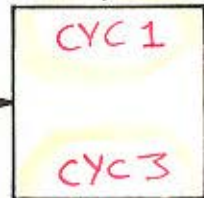
- P271. WHEN IF-1 LTH SETS, GATE IC TO PAB, AND SET PAA 60.
- P272. WHEN IF-2 LTH SETS, GATE PAL (40-63) TO IC.
- P18 3. RASCR μ -ORDER "ANDED" WITH IF-2 LTH SETS IF-1 TGR AND IF-1 LTH.
- M-PROG { 4. ISSUE MS REQ*D-3 FOR OPERAND.
- 5. E(02-07) \rightarrow ROA.

INCREASES IC BY 8

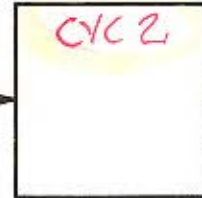
22

www.ibm360.info

098 (QK011)



408 (QK011)



8CE (QK011)

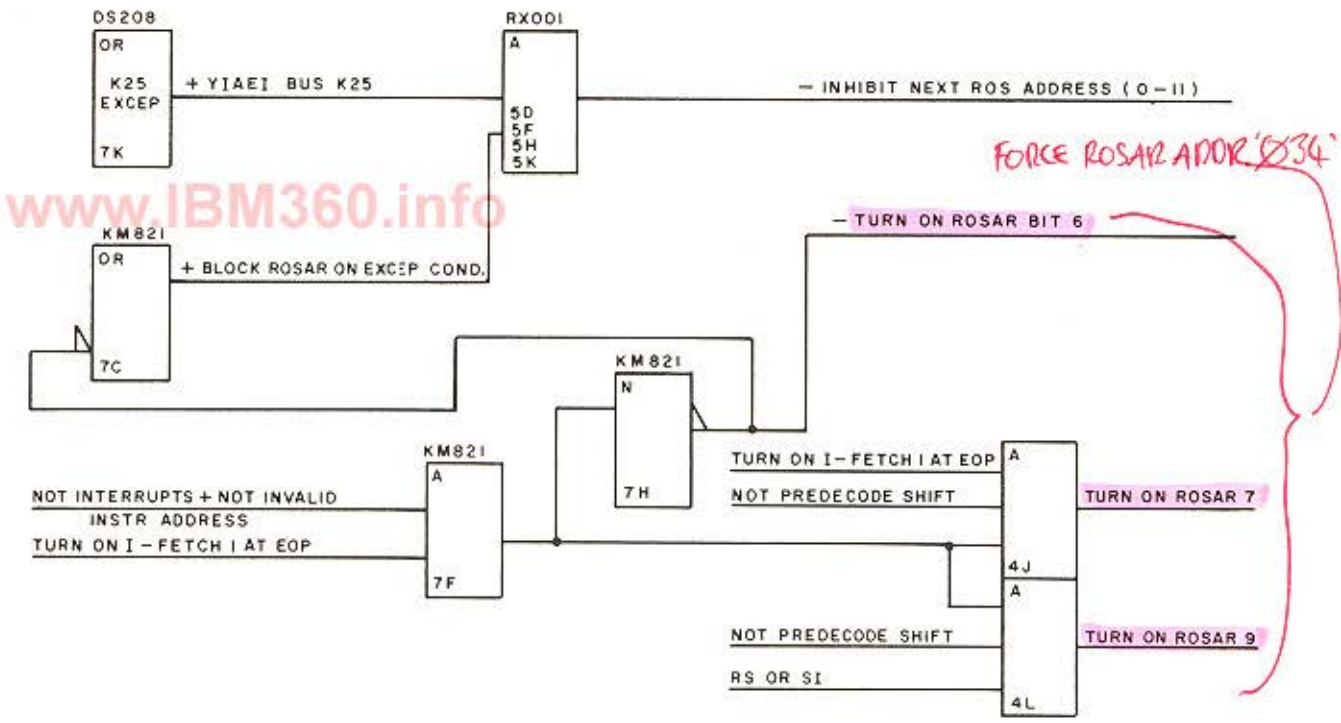


- P24 1. IF-3 LTH "ANDED" WITH IF-1 LTH GATES SDBO TO Q. - INSTR* D/WORD COMES FROM S.E.
- P25 2. ALSO GATES SDBO (00-15) TO R IF IC(21-22) = 00.

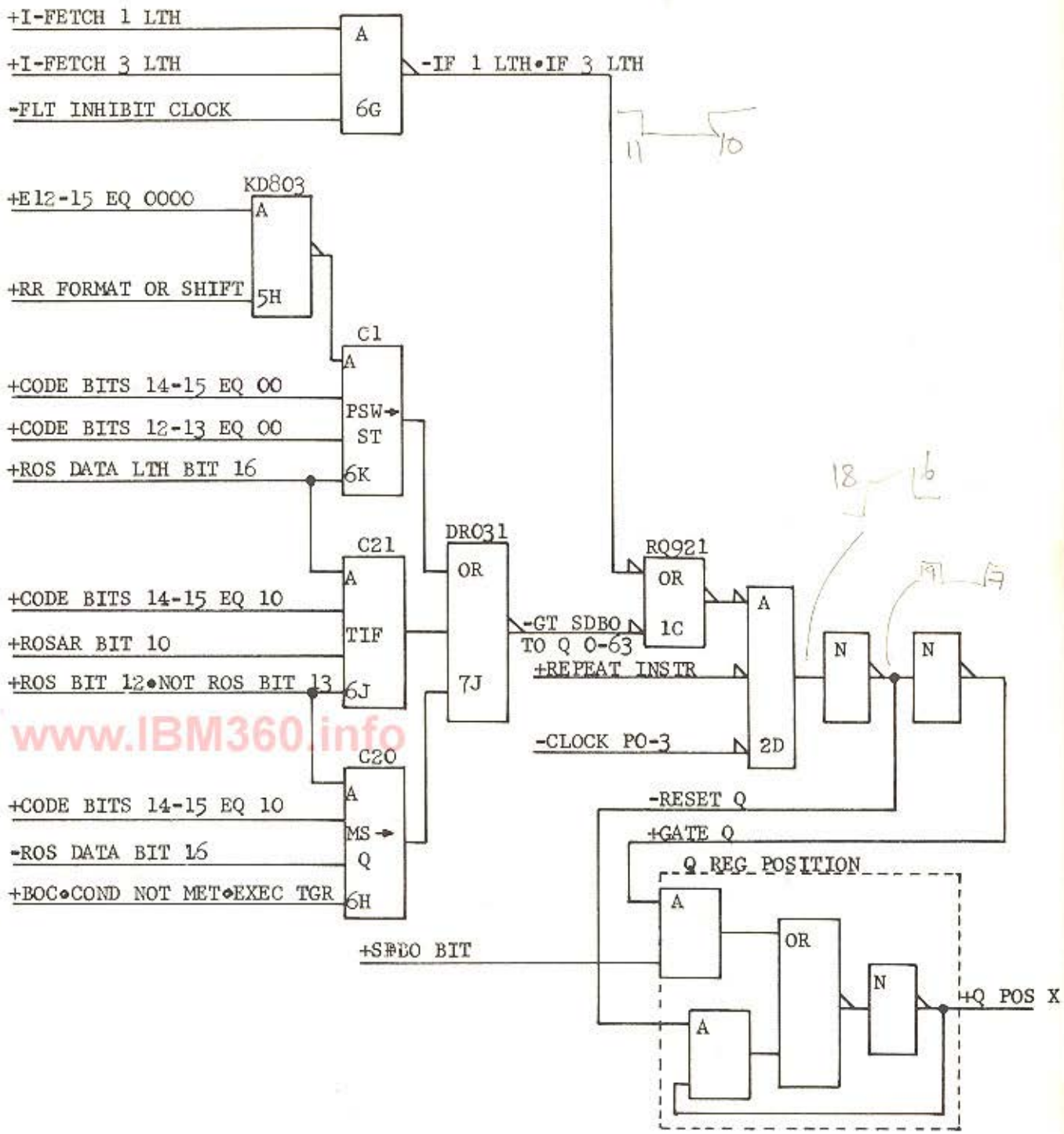
- 1. MS 1 \rightarrow T GATES SDBO (32-63) TO T. OPERAND

Flow Chart in AE-C-02 Page 111.

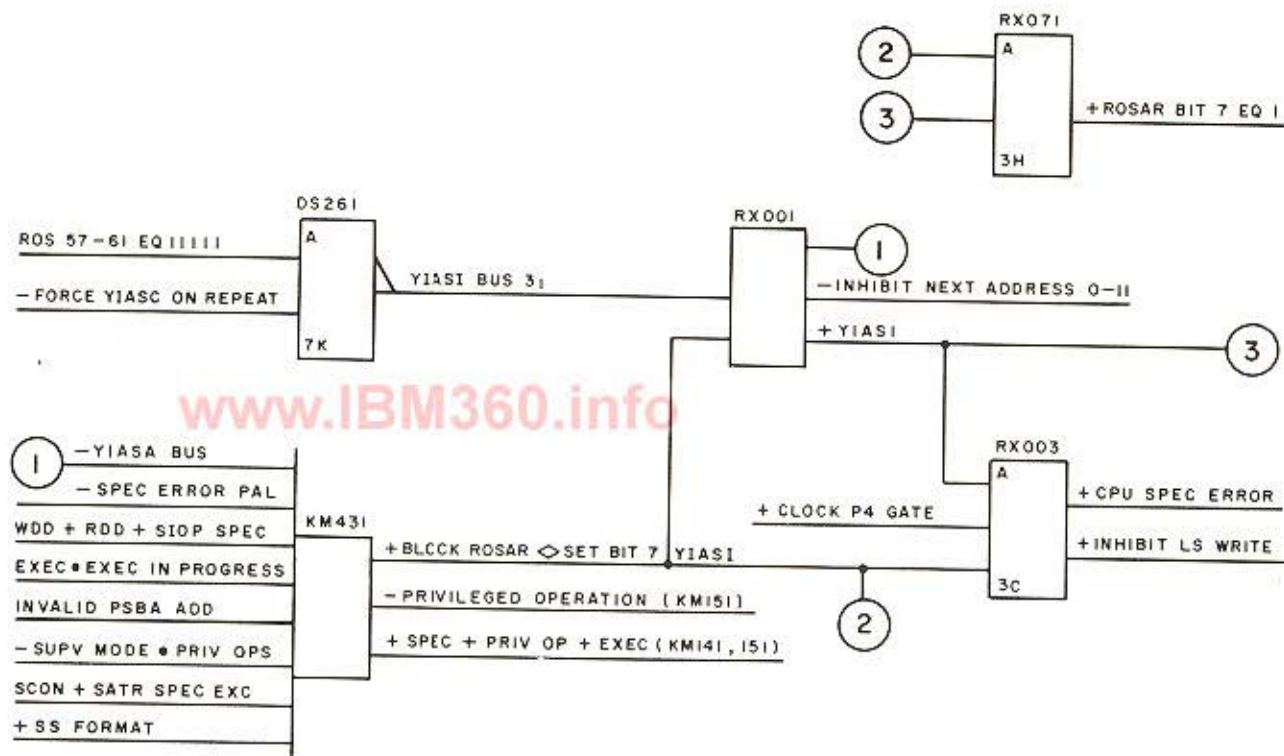
Q REFILL EXCEPTIONAL CONDITION (NEOP)



Exception μ -Order For "Q" Refill Priority (ROS 034) (RS-SI FORMAT)

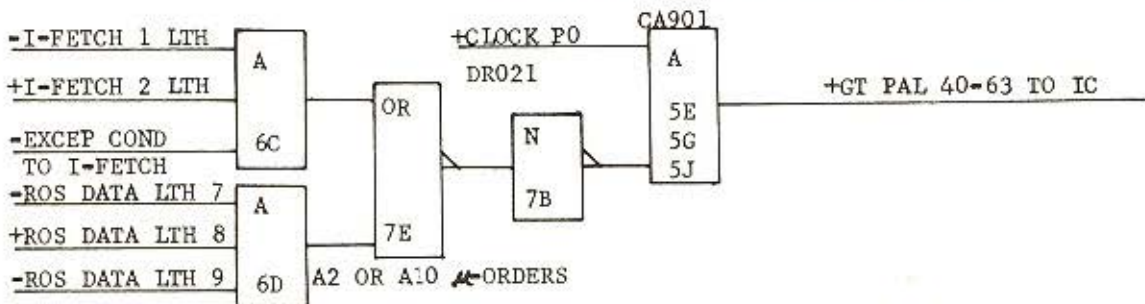
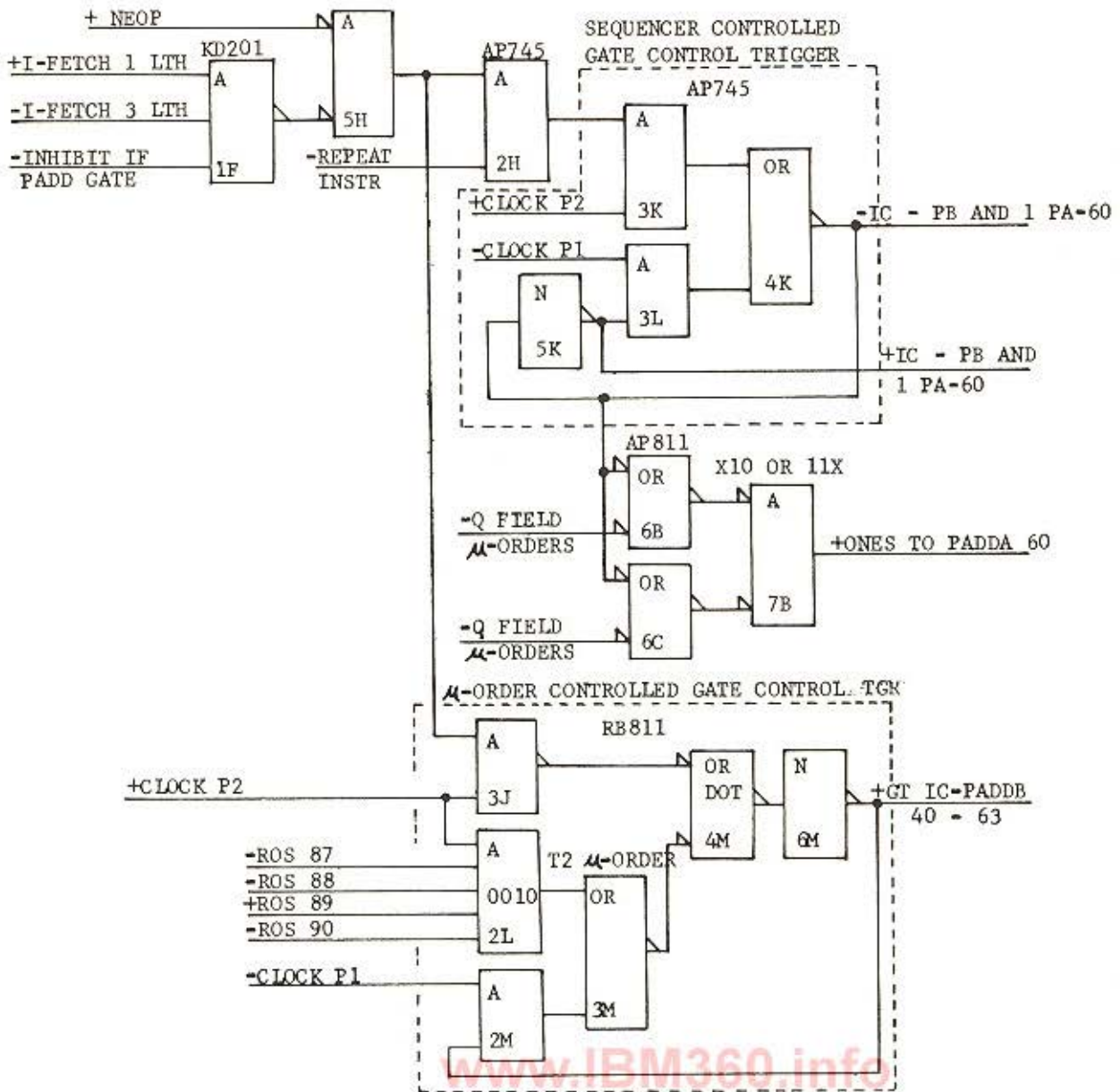


GATING SDBO TO Q REG.



SPEC μ -Order (K31) Force ROS to 010

2-12



GATING IC PLUS 8 TO PARALLEL ADDER TO IC.